Patents

Patents **1 - 10** on **configuration register, base address, pointer, size, input/output**. (**0.27** seconds)

Sort by relevance | Sort by date (new first) | Sort by date (old first)

System for assigning a received data packet to a data communications channel ...
US Pat. 5948080 - Filed Apr 25, 1997 - Texas Instruments Incorporated
Local bus interface logic 70 provides a group of special **input/output** ports .... **Pointer** dual-port **address** mapping logic 86 uses the three **size** values from ...

System for controlling data packet transfers by associating plurality of ...
US Pat. 6006286 - Filed Mar 6, 1997 - Texas Instruments Incorporated
The auxiliary interface is a generic **input/output** port that may be accessed through a third PCI memory-based **address register** within PCI **configuration** ...

System for writing a plurality of data bits less than from the total number ...
US Pat. 5996032 - Filed Apr 17, 1997 - Texas Instruments Incorporated
PCI **configuration** control and status **register** 68 includes a timer bit for ... Otherwise, this space is available as part of the auxiliary **address base** in ...

Method and system for assigning a direct memory access priority in a ...
US Pat. 5983301 - Filed Apr 29, 1997 - Texas Instruments Incorporated
The auxiliary interface is a generic **input/output** port that may be accessed through a third PCI memory-based **address register** within PCI **configuration** ...

Packet data transferring system for autonomously operating a DMA by ...
US Pat. 6081852 - Filed Apr 29, 1997 - Texas Instruments Incorporated
The auxiliary interface is a generic **input/output** port that may be accessed through a third PCI memory-based **address register** within PCI **configuration** ...

Method and system for extracting control information from packetized data ...
US Pat. 6333938 - Filed Apr 29, 1997 - Texas Instruments Incorporated
The auxiliary interface is a generic **input/output** port that may be accessed through a third PCI memory-based **address register** within PCI **configuration** ...

Configuration management method for hot adding and hot replacing devices
US Pat. 6148355 - Filed Oct 1, 1997 - Micron Electronics, Inc.
Under the PCI **configuration** standard, if the low order bit of a **base address register** is set, then that **base register** represents an I/O **address** and the ...

Efficient data transfer mechanism for **input/output** devices
US Pat. 6049842 - Filed May 1, 1997 - International Business Machines Corporation
Three **configuration** registers 26 are associated with each queue. For each queue one **register** holds the **base address** in main memory of the queue. ...

Method for using computer system memory as a modem data buffer by ...
US Pat. 6134609 - Filed Mar 31, 1998 - Micron Electronics, Inc.
2, particular embodiments of the modem **input/output** 24, the memory/modem interface

... **register** 56 stores a memory **address pointer** value associated with the ...

Register window system for reducing the need for overflow-write by ...
US Pat. 5233691 - Filed Dec 13, 1989 - Mitsubishi Denki Kabushiki Kaisha
4 is a schematic diagram showing a relationship to point the **base address** of the following/preceding among each **pointer**, each **register** window, ...

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Result Page: 1 2 3 **Next**

Patents Patents **1 - 4** on **configuration register, base address, pointer, predetermined size, input/output**. (**0.22**

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System for assigning a received data packet to a data communications channel ...
US Pat. 5948080 - Filed Apr 25, 1997 - Texas Instruments Incorporated
Local bus interface logic 70 provides a group of special **input/output** ports .... **Pointer** dual-port **address** mapping logic 86 uses the three **size** values from ...

Efficient data transfer mechanism for **input/output** devices having a device ...
US Pat. 6338102 - Filed Oct 19, 1999 - International Business Machines Corporation
Three **configuration** registers 26 are associated with each w queue. For each queue one **register** holds the **base address** in main memory of the queue. ...

Television receiver, video signal processing device, image processing device ...
US Pat. 6353460 - Filed Sep 29, 1998 - Matsushita Electric Industrial Co., Ltd.
10 The memory **address** generated by the **address** generation function of the write **pointer register** 2058 is supplied to the 2o **address** terminal of the SDRAM ...

Processor for a graphic terminal
US Pat. 4266253 - Filed May 16, 1979 - Thomson-CSF
22 shows the **input/output** means of the data bus MPDB. FIG. 23 shows the means for decoding the **address** words. FIGS. 24a and 246 show the means for ...

Direct memory access transfer reduction method and apparatus to overlay data ...

Patrick L. Connor et al

Patents Patents **1 - 7** on **configuration register, base address, pointer, predetermined value, input/output**. (**0.2**

Sort by relevance | Sort by date (new first) | Sort by date (old first)

System for assigning a received data packet to a data communications channel ...
US Pat. 5948080 - Filed Apr 25, 1997 - Texas Instruments Incorporated
Otherwise, this space is available as part of the auxiliary **address base** in the ... Each **pointer** counts in the range from 0 to its fifo size **value** minus 1. ...

Efficient data transfer mechanism for **input/output** devices having a device ...
US Pat. 6338102 - Filed Oct 19, 1999 - International Business Machines Corporation
Three **configuration** registers 26 are associated with each w queue. For each queue one **register** holds the **base address** in main memory of the queue. ...

Television receiver, video signal processing device, image processing device ...
US Pat. 6353460 - Filed Sep 29, 1998 - Matsushita Electric Industrial Co., Ltd.
10 The memory **address** generated by the **address** generation function of the write **pointer register** 2058 is supplied to the 20 **address** terminal of the SDRAM ...

Direct memory access controller and method therefor
US Pat. 6421744 - Filed Oct 25, 1999 - Motorola, Inc.
A **register** within the DMA, referred to as a "TASKBAR" or task table **base** ... table **pointer**, a function descriptor **base address**, **configuration** bit(s), ...

Reconfigurable expert rule processing system
US Pat. 6314416 - Filed Nov 17, 1998 - Interface & Control Systems, Inc.
Each allocated **register** is designated by unique **address** information such that ... at random by use of a software **pointer**, and to do so up to bits at a time. ...

Processor for a graphic terminal
US Pat. 4266253 - Filed May 16, 1979 - Thomson-CSF
22 shows the **input/output** means of the data bus MPDB. FIG. 23 shows the means for decoding the **address** words. FIGS. 24a and 246 show the means for ...

Platform and method for issuing and certifying a hardware-protected ...
US Pat. 6996710 - Filed Mar 31, 2000 - Intel Corporation
For that case, a **pointer** to the beginning of a memory array in the unprotected ... The protected memory 152 further contains a **predetermined address** space ...

EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	1	("5909557").PN.	US-PGPUB; USPAT; USOCR	OR	OFF	2007/11/06 08:52
L2	1	"5671355".PN.	USPAT; USOCR	OR	ON	2007/11/06 08:53
L3	1	"5623687".PN.	USPAT; USOCR	OR	ON	2007/11/06 08:59
L4	1	"5594874".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:01
L5	1	"5537601".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:02
L6	1	"5428748".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:02
L7	1	"5371892".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:05
L8	1	"5140691".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:03
L9	1	"5361365".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:04
L10	1	"5185516".PN.	USPAT; USOCR	OR	ON	2007/11/06 09:04
L11	34	"5371892".uref.	USPAT; USOCR	OR	ON	2007/11/06 09:14